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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,136	10/21/2003	Ming Fang	42P17278	6592

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EXAMINER	
BEREZNY, NEMA O	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 11/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/691,136	FANG ET AL.	
	Examiner	Art Unit	
	Nema O Berezny	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) *15-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 31-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to Applicant's Amendment filed 9-2-04, which has been entered and considered. Claims 1-38 are currently pending.

Election/Restrictions

Applicant's election of claims 1-14 in the reply filed on 9-2-04 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-6, 10, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schwiebert et al. (5,672,542) in view of Kato et al. (5,394,490). Schwiebert discloses a method, comprising: forming a die (Figs.3A-3H el.320) with a surface (el.321); forming conductive bumps on the surface of the die, wherein forming conductive bumps comprises: depositing a mask material layer (el.326) on the die; patterning the mask material layer to form pad openings (el.330); depositing a second conductive layer (el.334) in the pad openings of the patterned mask; and removing the

mask material (Figs.3C-3D); forming a substrate (el.350); and bonding the conductive bumps to the substrate (Fig.3G). However, Schwiebert does not disclose a waveguide. Schwiebert would look to one such as Kato for easy integration because Kato discloses conductive bumps (Figs.1-2, 16-17 el.4) having a height equal or greater than the height of a waveguide (el.5; col.20 lines 14-18). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the waveguide of Kato with the method of Schwiebert since the optical waveguide interconnections easily integrate with flip chip electrodes (Kato - col.3 lines 56-65) **[claim 1]**.

Based upon the rejection of claim 1 above, Schwiebert also discloses wherein the conductive bumps have a height greater than about 80 micrometers, wherein the conductive bumps have a height in a range from 80 micrometers to about 120 micrometers, and wherein the conductive bumps have a height in a range from 95 micrometers to about 110 micrometers (col.5-col.6 table; col.5 lines 5-22) **[claims 3, 4, 5]**; wherein forming conductive bumps further comprises: depositing a first thin conductive layer (el.322) on the die; and depositing the mask material layer on the first thin conductive layer (Figs.3B-3C) **[claim 6]**; wherein the conductive bumps are formed on a plurality of dies that are part of a wafer (col.4 lines 50-52) **[claim 10]**; and wherein the first conductive layer comprises at least one of Ti, TiN, Cr, Ta, Ni, NiV, Co, Cu, Au, and Ag (col.4 lines 50-55) **[claim 32]**.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schwiebert in view of Kato as applied to claim 1 above, and further in view of Bakir et al.

(2003/0206680). Schwiebert in view of Kato do not disclose a specific waveguide height. However, Schwiebert and Kato would look to one such as Bakir for size compatibility because Bakir discloses wherein the waveguide has a height in a range of about 95 micrometers to about 110 micrometers (p.5 para.69). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the waveguide height of Bakir with the method of Schwiebert and Kato since Schwiebert and Kato would look to a waveguide device height that was close to but slightly less than the height of the conductive bumps, as evidenced by Fig.1 of Kato.

Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schwiebert in view of Kato as applied to claims 1 and 6 above, and further in view of Berndlmaier et al. (5,059,553). Schwiebert in view of Kato do not disclose a protection layer or a barrier layer. Schwiebert and Kato would look to one such as Berndlmaier for oxidation and corrosion resistance because Berndlmaier discloses depositing a protection layer (Fig.2 el.44) on a conductive layer **[claim 7]**; and depositing a barrier layer (el.38; col.3 lines 54-65) between the protection layer and the conductive layer **[claim 8]**. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the protection and barrier layers of Berndlmaier with the method of Schwiebert and Kato in order to provide oxidation resistance and corrosion resistance, respectively.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schwiebert, Kato, and Berndlmaier as applied to claims 1, 6, and 7 above, and further in view of Brandenburg (5,770,477). Schwiebert, Kato, and Berndlmaier do not disclose a fluxless soldering process. However, Schwiebert, Kato, and Berndlmaier would look to one such as Brandenburg for precise bump positioning because Brandenburg discloses wherein bonding the conductive bumps to the substrate comprises bonding the conductive bumps to the substrate with a fluxless soldering process (col.3 lines 60-65). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the fluxless soldering of Brandenburg with the method of Schwiebert, Kato, and Berndlmaier in order to precisely deposit the solder wherein each bump will be accurately mated with a corresponding conductor after reflowing (Brandenburg – col.3 line 66 – col.4 line 5).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schwiebert in view of Kato as applied to claims 1 and 10 above, and further in view of Pendse (2004/0070080). Schwiebert in view of Kato do not disclose singulating the die from a wafer after forming the conductive bumps. However, Schwiebert and Kato would look to one such as Pendse for economical mass fabrication because Pendse discloses singulating the die from the wafer after forming the conductive bumps (p.5 para.56). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the singulating of Pendse with the method of Schwiebert and

Kato in order to economically form a large plurality of dies on a wafer in one step, then singulate said dies from the wafer.

Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schwiebert in view of Kato as applied to claim 1 above, and further in view of Jimarez et al. (2001/0018230). Schwiebert and Kato do not disclose conductive bumps having a higher melting point than said bonding temperature of said conductive bumps to said substrate. However, Schwiebert and Kato would look to one such as Jimarez for easy reworkability because Jimarez discloses wherein the conductive bumps are bonded to the substrate at a bonding temperature and the conductive bumps have a melting point higher than the bonding temperature **[claim 12]**, and wherein the bonding temperature is at least a melting point of a solder material that bonds the conductive bumps to the substrate **[claim 13]**, and wherein the bonding temperature is about 230 degrees Celsius **[claim 14]** (p.4 para.63). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the bonding of Jimarez with the method of Schwiebert and Kato in order to provide easy reworkability (Jimarez - p.2 para.29).

Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schwiebert in view of Kato as applied to claim 1 above, and further in view of Makino el al. (6,566,239). Schwiebert and Kato do not disclose a second conductive layer comprising at least one of Cu, Ni, Co, Fe, Au, and Ag. However, Schwiebert and Kato

would look to one such as Makino for high electrical conductivity because Makino discloses a second conductive layer comprising at least one of Cu, Ni, Co, Fe, Au, and Ag (col.7 lines 65-67). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the conductive layer of Makino with the method of Schwiebert and Kato because copper provides a high level of electrical conductivity and low electrical resistance (inherent property of copper).

Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schwiebert, Kato, and Berndlmaier as applied to claims 1, 6, and 7 above, and further in view of Makino et al. (6,566,239). Schwiebert, Kato, and Berndlmaier do not disclose a protection layer comprising at least one of Au, Pt, Pd, Ag, Ir, Os, Ru, and Rh. However, Schwiebert, Kato, and Berndlmaier would look to one such as Makino for oxidation resistance because Makino discloses a protection layer comprising at least one of Au, Pt, Pd, Ag, Ir, Os, Ru, and Rh (col.8 lines 18-19). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the protection layer of Makino with the method of Schwiebert, Kato, and Berndlmaier in order to provide an oxidation inhibiting layer (Makino - col.8 lines 19-20).

Claims 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Makino et al. (6,566,239) in view of Kato et al. (5,394,490). Makino discloses a method, comprising: forming a plurality of conductive bumps on a surface of a die, wherein forming the conductive bumps comprises: depositing a first thin conductive layer

(Figs.13-24 el.44) on the die (el.41); depositing an unpatterned layer of mask material on the first thin conductive layer (col.6 lines 58-60); patterning the layer of mask material to form a plurality of trenches (el.46) through the mask material to the first thin conductive layer (Fig.16); depositing a second conductive layer (el.47) in the trenches; removing substantially all the mask material after depositing the second conductive layer (Figs.17-18); and removing substantially all of the first thin conductive layer except for portions of the first thin conductive layer beneath the second conductive layer (Figs.18-19). However, Makino does not disclose a waveguide. Makino would look to one such as Kato for easy integration because Kato discloses bonding conductive bumps (Figs.1,2 el.4) to a substrate (el.2) with a waveguide (el.5) between the substrate and the die wherein the waveguide is not located within a trench in the surface of the substrate, and wherein the conductive bumps have a height greater than a height of the waveguide (Fig.1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the waveguide of Kato with the method of Makino in order to easily integrate optical waveguide interconnections with flip chip electrodes (Kato – col.3 lines 56-65).

Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Makino in view of Kato as applied to claims 34-35 above, and further in view of Bakir et al. (2003/0206680). Makino in view of Kato do not disclose a waveguide height. However, Makino and Kato would look to one such as Bakir for size compatibility because Bakir discloses wherein the waveguide has a height in a range of about 95 micrometers to

about 110 micrometers (p.5 para.69). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the waveguide height of Bakir with the method of Makino and Kato since Makino and Kato would look to a waveguide device height that was close to but slightly less than the height of the conductive bumps, as evidenced by Fig.1 of Kato.

Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Makino in view of Kato as applied to claim 34 above, and further in view of Jimarez et al. (2001/0018230). Makino and Kato do not disclose conductive bumps having a higher melting point than said bonding temperature of said conductive bumps to said substrate. However, Makino and Kato would look to one such as Jimarez for easy reworkability because Jimarez discloses wherein the conductive bumps are reflow soldered and bonded to the substrate at a bonding temperature and the conductive bumps have a melting point higher than the bonding temperature (p.4 para.63). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the bonding of Jimarez with the method of Makino and Kato in order to provide easy reworkability (Jimarez - p.2 para.29).

Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Makino in view of Kato as applied to claim 34 above, and further in view of Schwiebert et al. (5,672,542). Makino and Kato do not disclose a second conductive layer having a thickness between about 70 micrometers and about 120 micrometers. However,

Makino and Kato would look to one such as Schwiebert for achieving a final ball height because Schwiebert discloses a second conductive layer having a thickness between about 70 micrometers and about 120 micrometers (Fig.3B; col.6 lines 26-28). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the thickness of Schwiebert with the method of Makino and Kato since the thickness of the second conductive layer determines the desired final ball height (Schwiebert - col.5 lines 5-22).

Response to Arguments

Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nema O Berezny whose telephone number is (571) 272-1686. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NB

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